CPS-JK12

SHEET INDEX

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SYMBOL

BUFFER C
ELEMENT IDENT
A

TERM. MOD.	FUNCT	TERM.	LOC
CLKITRO	I	015	2A3
ENDTO	I	104	2A0
LDITR1	I	004	2A6
LBADO	I	106	2A7
SDITRO	I	002	2A0
SWIFT1	I	014	2A3
PM48	I	217,317	2A9
LDDO	Ø	017	2G9
LOD1	Ø	115	2G9
PPEHO	Ø	103	2N3
PPELO	Ø	114	2H7
-17.2DV	Ø	018,118	2G9
INFPHO	ØI	101	2N3
INFPLO	ØI	005	2H6
INFOOO	ØI	116	2H6
INFO1O	ØI	216	2H6
INFO2O	ØI	016	2N5
INFO3O	ØI	315	2H5
INFO4O	ØI	113	2H4
INFO5O	ØI	215	2H4
INFO6O	ØI	013	2H4
INFO7O	ØI	214	2H4
INFO8O	ØI	006	2H2
INFO9O	ØI	207	2H2
INF100	ØI	105	2H2
INF110	ØI	305	2N2
INF120	ØI	003	2H1
INF130	ØI	203	2N1
INF140	ØI	102	2N1
INF150	ØI	301	2H0
+5	P	000,119	2G7
GRD	G	200,319	2G8

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	NFA DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IN

CURRENT DRAIN: +5V SUPPLY = 325mA
-48V SUPPLY = 50mA

NOTES:

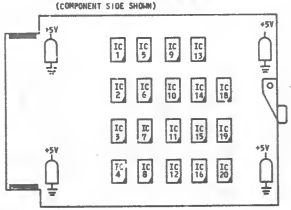
1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD TERM.
41AE	16	7,8
41BP	16	8
41CA	16	8
41CF	16	7,8
41DA	16	7,8
41EF	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.
6. INTEGRATED CIRCUIT LOCATION GUIDE: (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK12
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE.	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE

DWG ISS OR CTR ISSUED	DATE ISSUED	BY	APPD
1	—	10-8-74	KWF LRE WTS LAE RPG
2D1	—	1-5-76	APPR LILT LRE LAE RPG

ISSUE 2D1

IN98

JK12 CIRCUIT PACK

BUFFER C CIRCUIT

AT&TCO STANDARD

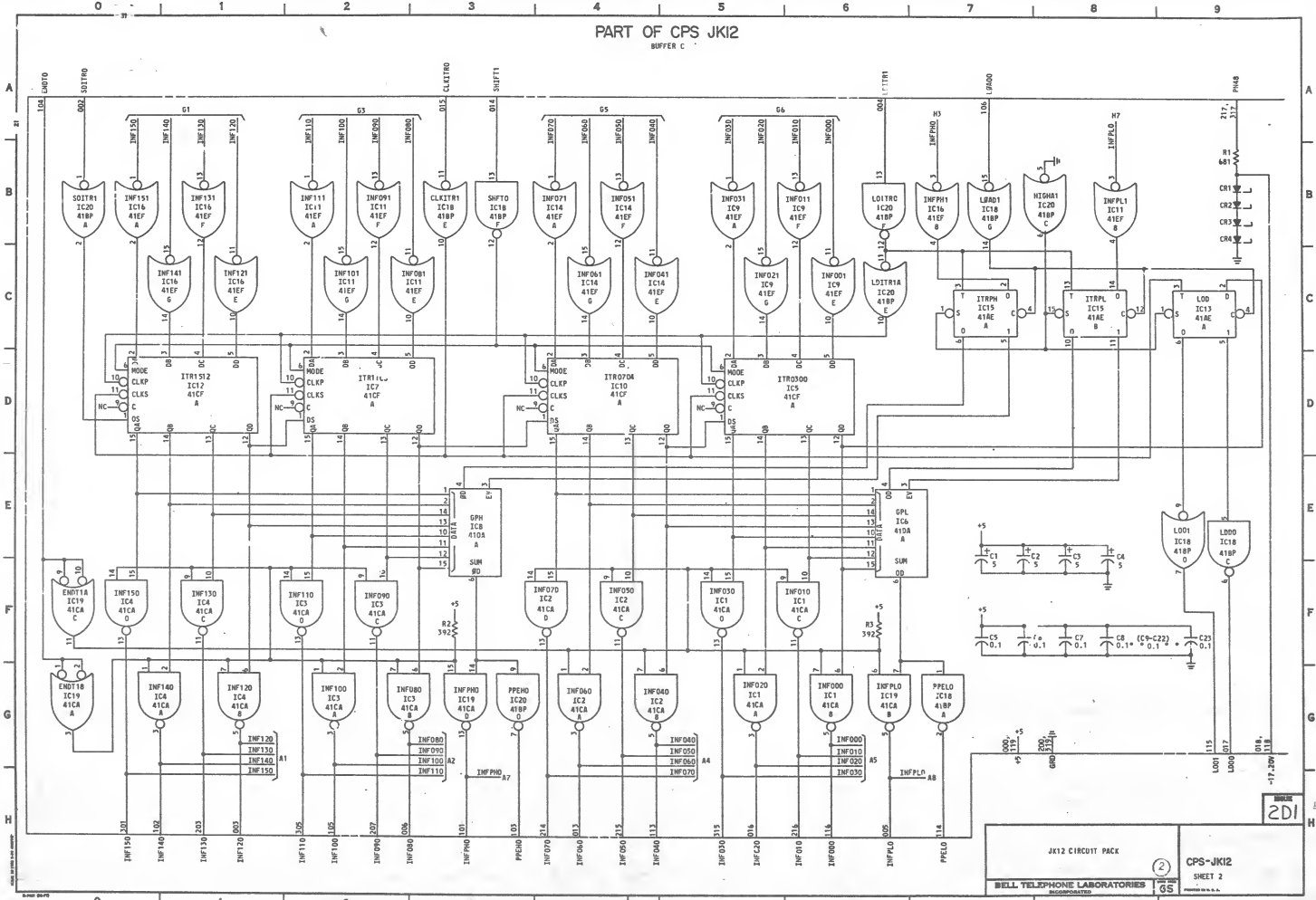
(2)

CPS-JK12
3 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED

SIZE CODE 65

CPS-JK12


PART OF CPS JK12
BUFFER C
BELL TELEPHONE LABORATORIES INCORPORATED
JK12 CIRCUIT PACK
CPS-JK12
SHEET 2
2D1

PART OF CPS JK12

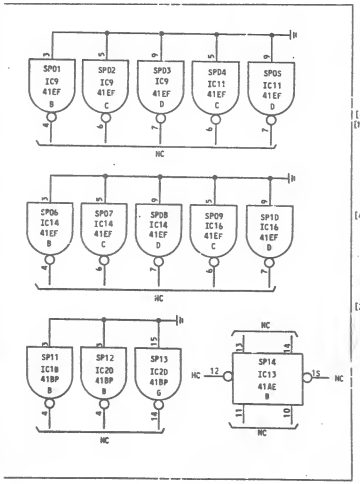
BUFFER C

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 41CA DESIG	SH LOC	IC2 41CA DESIG	SH LOC	IC3 41CA DESIG	SH LOC	IC4 41CA DESIG	SH LOC	IC5 41CF DESIG	SH LOC	IC6 41DA DESIG	SH LOC	IC7 41CF DESIG	SH LOC	IC8 41DA DESIG	SH LOC	IC9 41EF DESIG	SH LOC	IC10 41CF DESIG	SH LOC	IC11 41EF DESIG	SH LOC
A	INFD20	2G5	INFD6D	2J4	INFD0D	2G2	INF14D	2G1	ITRD300	2D6	GPL	2E6	ITR1108	2D2	GPH	2E3	INFD31	2B5	ITRD704	2D4	INF111	2B2
B	INFD00	2G6	INFD4D	2G4	INFD8D	2G2	INF12D	2G1									SPD1	3E0			INFPL1	2B8
C	INFD1D	2F6	INFD5D	2F4	INFD9D	2F2	INF13D	2F1									SPD2	3ED			SP04	3E1
D	INFD3D	2F5	INFD7D	2F4	INF11D	2F2	INF15D	2F0									SPD3	3E1			SP05	3E1
E																	INFD01	2C6			INF081	2C3
F																	INFD11	2B6			INF091	2B2
G																	INFD21	2C5			INF101	2C2

LOC CODE ELEM ID	IC12 41CF DESIG	SH LOC	IC13 41AE DESIG	SH LOC	IC14 41EF DESIG	SH LOC	IC15 41AE DESIG	SH LOC	IC16 41EF DESIG	SH LOC	IC18 41BP DESIG	SH LOC	IC19 41CA DESIG	SH LOC	IC20 41BP DESIG	SH LOC
A	ITR1512	2D1	LDD	2C9	INFD71	2B4	ITRPH	2C7	INF1S1	2B0	PPELD	2G7	EHDT1B	2G0	SDITR1	2B0
B			SP14	3G1	SP06	3FD	ITRPL	2C8	INFFH1	2B7	SP11	3G0	INFPLD	2G6	SP12	3G0
C					SP07	3FD			SPD9	3F1	LDDO	2E9	ENDT1A	2FD	HIGHA1	2B8
D					SP08	3F1			SP1D	3F1	LDD1	2E9	INFPHO	2G3	PPEHD	2G3
E					INFD41	2C4			INF121	2C1	CLKITR1	2D3			LDITR1A	2C6
F					INFD51	2B4			INF131	2B1	SHFTD	2B3			LDITRD	2B6
G					INFD61	2C4			INF141	2C1	LBAD1	2B7			SP13	3G1



CAPACITOR

DESIGN	CODE
[4]C1-C4	601A,5
[9]C5-C23	KS-19774 L5,D.1

DIODE

DESIG	CODE
[4]CR1-CR4	448B

RESISTOR

DESIG	CODE
R1	KS-14603 L6,681
[2]R2,R3	KS-20616 L1A,392

CIRCUIT DESCRIPTION:

THIS CIRCUIT PACK IS PART OF THE BUFFER UNIT. IT CONTAINS A 16-BIT SHIFT REGISTER FOR PARALLEL-TO-SERIAL AND SERIAL-TO-PARALLEL CONVERSION. TWO B-BIT PARITY TREES ARE USED TO CHECK AND GENERATE PARITY. THE SERIAL INPUT/OUTPUT LEADS CONNECT TO THE OFF-LINE SERIAL BUFFER ON JK13. PARALLEL INPUT AND OUTPUTS ARE CONNECTED TO THE BIDIRECTIONAL INFORMATION LEADS.

THE REGISTER IS NORMALLY IN THE PARALLEL LOAD MODE. THE MODE INPUT OF THE 41CFs ARE HELD HIGH BY THE SHFT1 INPUT BEING LOW. THE LBADD IS HIGH WHENEVER THE BUFFER UNIT IS NOT IN THE LOAD STATE. IN THIS MODE, THE PARITY F/F ITRPL AND ITRPH ARE HELD IN THE CLEARED STATE. THIS FORCES THE EVEN INPUTS OF THE PARITY TREES GPL AND GPH TO A LOW LEVEL AND THE ODD INPUTS TO A HIGH LEVEL. IN THIS PARITY GENERATION MODE, THE OUTPUTS OF THE PARITY TREES ARE HIGH FOR AN EVEN NUMBER OF ONE INPUTS OR ARE LOW FOR AN ODD NUMBER OF ONE INPUTS. THE TRUTH TABLE BELOW SHOWS THE OPERATION.

Σ OF INPUTS	INPUT EVEN	INPUT ODD	ODD OUT
ODD	0	1	0
EVEN	0	1	1

AN UNLOAD OPERATION IS DEFINED BY A 16-BIT DATA TRANSFER FROM THE OFF-LINE BUFFER TO THE 3A CC. THE FOLLOWING SEQUENCE IS PERFORMED ON JK12.

THE SERIAL DATA FROM THE OFF-LINE BUFFER APPEARS ON SDITRO. LEAD SHIFT1 IS SET HIGH TO PLACE THE 16-BIT REGISTER INTO THE SERIAL SHIFT MODE. SIXTEEN GROUND LEVEL PULSES ARE APPLIED TO LEAD CLKITRO. THE DATA IS SHIFTED INTO THE REGISTER AT THE TRAILING EDGE OF THE CLOCK PULSES. LEAD LDDO IS HELD AT A HIGH LEVEL. THIS MEANS THAT ZERO DATA IS SHIFTED INTO THE OFF-LINE BUFFER DURING UNLOAD OPERATIONS. THE 16-DATA BITS CONTAINED IN THE REGISTER ARE FED INTO THE PARITY TREES. THE PARITY TREES ARE ALLOWED TO SETTLE. THE SHFT1 LEAD IS SET LOW AGAIN TO PLACE THE REGISTER INTO THE PARALLEL LOAD MODE. THE CONTENTS OF THE REGISTER AND THE TWO PARITY BITS ARE THEN GATED ONTO THE INFORMATION BUS LEADS BY SETTING LEAD ENDTO TO A LOW LEVEL.

CIRCUIT DESCRIPTION (CONT):

LBAD

A LOAD OPERATION IS DEFINED BY A 16-BIT DATA TRANSFER FROM THE CC TO THE OFF-LINE BUFFER. THE FOLLOWING SEQUENCE IS PERFORMED ON JK12. WHEN THE LBAD STATE IS SET, LEAD LBADO IS AT GROUND LEVEL REMOVING THE CLEAR INPUT FROM ITRPH, ITRPL, AND LDD1 F/Fs. SIXTEEN BITS OF INFORMATION AND THE TWO PARITY BITS APPEAR IN PARALLEL ON THE INFORMATION BUS LEADS. A SINGLE HIGH LEVEL PULSE APPEARS ON LEAD LDITR1. THE STATE OF THE INFORMATION LEADS IS CLOCKED INTO THE REGISTER AND THE TWO PARITY F/F AT THE TRAILING EDGE OF THE PULSE. IN THE LOAD MODE, THE TWO PARITY TREES AND THE TWO PARITY F/F CHECK FOR PROPER PARITY OF THE JUST RECEIVED DATA WORD. AN ERROR CONDITION IS INDICATED WHENEVER PPELD OR PPEHD IS AT GROUND LEVEL. THE FOLLOWING TRUTH TABLE SHOWS THE CHECKING OPERATION.

Σ OF INPUTS	PARITY BITS	INPUT PDP	INCL. EVEN	PDD OUTPUT	
EVEN	1	D	1	D	NO ERROR
ODD	D	1	D	D	NO ERROR
ODD	1	D	1	1	ERROR
EVEN	D	1	D	1	ERROR

IF AN ERROR CONDITION EXISTS, NO SERIAL SHIFTING INTO THE OFF-LINE BUFFER TAKES PLACE. IF NO ERROR CONDITION EXISTS LEAD SHFT1 IS SET HIGH TO PLACE THE REGISTER INTO THE SERIAL SHIFT MODE. SIXTEEN CLOCK PULSES ON LEAD CLKITRO SHIFT THE 16-BIT WORD INTO THE OFF-LINE BUFFER VIA LEAD LDDO. F/F LDD1 IS CLOCKED ON THE LEADING EDGE OF CLKITRO AND THE REGISTER IS SHIFTED ON THE TRAILING EDGE. THE LDDO F/F KEEPS THE DATA STEADY OVER THE TRAILING EDGE OF THE OFF-LINE SHIFT PULSE ON JK13.

ISSUE 2D1

JK12 CIRCUIT PACK (2) CPS-JK12 SHEET 3

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CPS-JK12